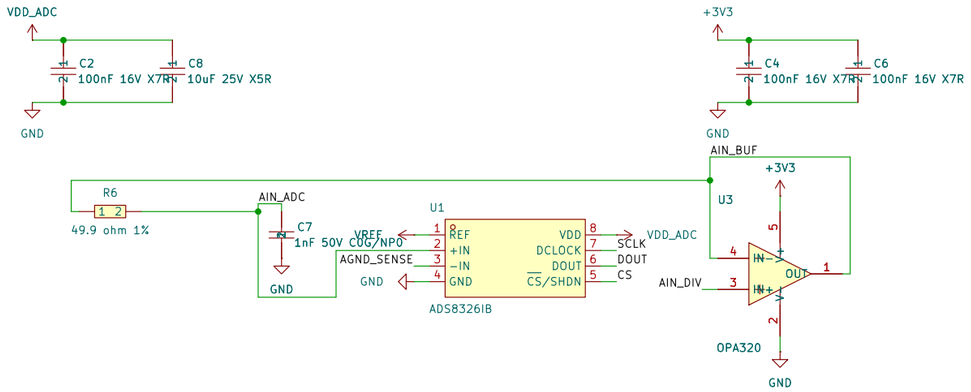
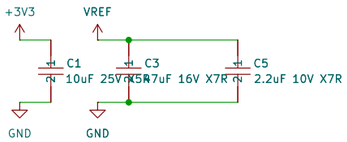
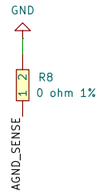
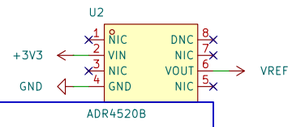


/AGND_SENSE — the −IN sense run: U1 pin 3 to R5's bottom pad, tied to GND ONLY through R8









NOTE 1 THE SENSE IS ITS OWN NET. /AGND_SENSE has exactly three nodes — U1 pin 3 (−IN), R5's bottom pad, R8 — and R8 (0 ohm) is the ONE tie to GND, at the string bottom. U1 pin 3 must NEVER carry a GND label or a GND symbol, and no second tie may be added anywhere. A PART and not a label because a divider passes a ground offset at UNITY while dividing the signal by K = 0.400 (1 mV between string bottom and converter = 2.5 mV at the terminal, half the 25 degC budget), and on a shared GND net the B.Cu pour would tie pin 3 to the pour AT THE CONVERTER just as it ties pin 4. Split, the reading is K*(V_sig − V_S) + Vos — the only residual is the J1-return-to-string-bottom pour offset, at UNITY, carrying just the string's 5 uA: sub-1 uV. −IN sits −0.25 uV off U1 GND through R8, six orders inside the −0.3/+0.5 V window. P7: keep the run dedicated.
NOTE 2 The guard ring around /AIN_DIV and U3 +IN is P7 COPPER on /AIN_BUF (the buffer OUTPUT), never on /AIN_DIV itself. No schematic element.
NOTE 3 R7 + C2 + C8 are the ADS8326's own recommended rail entry (figs 44/45): R7 upstream of both caps, C2 the smaller and closest to the pin. It isolates U1 ALONE — U2 and U3 stay upstream on +3V3. No ferrite.
NOTE 4 NO series resistor between U2 VOUT and C3 / U1 REF (recorded ruling): a SAR's reference current varies with input code, so a series R becomes a code-dependent nonlinearity. C5 >= 1 uF is MANDATORY — the ADR4520's 1–100 uF load-capacitance window is two-ended.
NOTE 5 R1–R5 are FIVE EQUAL 200 k elements in ONE string tapped 3:2 (K = 0.400, Rtot 1.00 Mohm, tap Thevenin 240 kohm). Do not collapse.
NOTE 6 *** J2 MIS-MATE IS DESTRUCTIVE AND UNPROTECTED: pin 1 = +3V3 and pin 6 = GND, so a 180 degree reversal shorts the host's rail to its own ground through the cable. No series protection, no reverse diode, no keyed housing — all excluded by the scope tier. P6 must silk a pin-1 marker and a 1.6 legend. ***
NOTE 7 HOST POWER-UP: wait >= 50 ms after +3V3 before trusting a conversion. The reference settles in 90 us typ, but slew-limited charging of the ~49.2 uF on VREF at its 10 mA source limit is ALREADY 7–10 ms — a 10 ms wait has ~1x margin; 50 ms restores the 5x it was meant to carry.





J2 PIN 1 = +3V3 — 180 deg mis-mate shorts the host rail to its ground (unprotected)



ai-ee

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Title: bb-adc 0–5V precision front end -> 16-bit SPI SAR (ADS8326IB)

Size: A3	Date: 2026-08-17	**Rev: A**
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