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AD8226's 2 ohm REF rule: met at DC and low frequency (B9: 0.43 mohm DC, 0.17 ohm at 60 Hz),

crossed above ~700 Hz - harmless, Q1's common mode is STATIC. Numbers in the box.



STAGE-2 GAIN SET R5 RETURNS TO /VREF, NOT GND - that is what makes the pedestal EXACT

POWER +3V3 arrives at J3; C2 10uF bulk at J3; C1/C3 100nF at pin 8 of U1/U2 (AD8226 Fig.61, OPA2333 p15)

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bp_amp - BRIDGE FRONT END ON ONE 3.3 V RAIL  (architecture/blocks.md)
TRANSFER FUNCTION
  Vout = Vref + G1*G2*Vdiff      G1*G2 = 139.2 V/V,  Vref = 0.252 V
  Vout(-1 mV) = 0.113 V     Vout(0) = 0.252 V     Vout(+20 mV) = 3.037 V
  +25 mV overload clips at (V+) - 0.05 V and recovers, no fold-back.

GAIN SPLIT  G1 * G2 = 39.90 * 3.49
  G1 = 1 + 49.4k/RG = 1 + 49.4k/1.27k = 39.90   U1 AD8226, R1 across pins 2-3
  G2 = 1 + R4/R5    = 1 + 24.9k/10.0k = 3.49    U2B, OPA2333 half B
WHY IT IS SPLIT: the AD8226's INPUT VOLTAGE RANGE section (Eq.1-3, Table 8)
limits the internal 1st/2nd-stage nodes, not the pins.  Eq.2 ceiling on
|G*Vdiff| and the gain it allows at 20 mV FS (blocks.md Ruling 2) - note
which Vcm each row belongs to:
    Vcm 1.65 V (Q1), rail -5 %, 0 degC ..... 1.49 V   G <= 75
    Vcm 1.7325 V, rail -5 % AND excitation +5 % ..... 1.33 V   G <= 66
1.65 V is the stated operating point; the 1.33 V / G <= 66 pair is the
WORST CORNER, not the nominal common mode.  Either way a single stage at
G = 139 saturates INSIDE the part while its input and its output both
still look legal.  The data sheet's own remedy: less gain in the in-amp,
the rest later in the chain.

PEDESTAL   Vref = 3.3 V * R3/(R2+R3) = 3.3 * 10.0k/131.0k = 0.2519 V
   C4 filters the DIVIDER node (Thevenin 9.24k -> 172 Hz corner), never the
   buffer output - a follower into a capacitive load peaks.
   U2A buffers it.  AD8226 Fig.59 draws a bare divider into REF, crosses it
   out and marks it INCORRECT: source impedance at REF must stay below
   2 ohm, or the +IN path is amplified by 2(50k + Rref)/(100k + Rref) and
   CMRR collapses (9.24k there = -8.5 % error = -21 dB of CMRR left).

  HOW WELL THE BUFFER MEETS THAT RULE IS MEASURED, NOT FLAT (bench B9):
     DC 0.43 mohm     60 Hz 0.17 ohm     1 kHz 2.86 ohm     41 kHz 116 ohm
  Met through DC and the low frequencies where the AD8226 specifies CMRR;
  EXCEEDED above ~700 Hz (350 Hz on the pessimistic ro = 2 kohm bracket).
  Not a defect here - Q1 fixes the common mode at a STATIC 1.65 V with
  nothing at 1 kHz to convert, and the residual common-mode gain error is
  90.8 dB, at or above the part's own 90 dB min at 5 kHz.  A board with a
  MOVING common mode would have to rederive this.

*** R5 RETURNS TO /VREF, NOT TO GROUND ***
   U2B's + input sits at   V1 = Vref + G1*Vdiff.
   With R5 to /VREF:  Vout = V1 + (V1 - Vref)*R4/R5 = Vref + G1*G2*Vdiff.
   The output pedestal is therefore EXACTLY Vref - no matched network, no
   second reference node - and a shift of Vref lands on U1 REF and on the
   stage-2 return with OPPOSITE sign, so the reference's own drift and noise
   cancel to first order and survive only as the gain-1 pedestal term.
   With R5 to GND the pedestal would become G2*Vref and every bit of
   reference error would be amplified by G2.  A different, worse board.

/VREF IS ONE NODE WITH THREE LOADS: U2A OUT (1), U1 REF (6), R5.

J1 POLE ORDER IS IN- / IN+ / GND - LAYOUT DROVE THE PIN ASSIGNMENT.  J1 as
(IN+, IN-) against the AD8226's (-IN ... +IN) crosses the pair structurally
(P6 checked all 8 rotation/edge combinations).  Uncrossed costs 2 vias in
ONE leg - 0.6 pF, -123 dB at 1 kHz, inside budget - but they break the B.Cu
reference under the pair and unbalance the net whose symmetry is this
board's dominant error term.  Swapped: planar, symmetric, zero vias.
NOTHING ELECTRICAL MOVED - IN+ still lands on U1 pin 4 and "IN+ above IN-
gives positive out" holds.  THE SILK MUST SAY IN- / IN+ / GND.

SINGLE SUPPLY: U1 pin 5 (-VS) and U2 pin 4 (V-) go to GND.  The RRIO OPA2333
(30 mV typ from either rail) is the part that faces the rails, not the AD8226
(0.10 V guaranteed floor) - the same spec that makes a grounded REF unusable.

ACCURACY, RECORDED NOT SMOOTHED (blocks.md Ruling 3): Q7's 5 uV RTI over
0-50 degC is 10 ppm of full scale per degC and is NOT met - 13.9 uV typ /
56.4 uV max offset drift, plus 30-87 uV of gain drift at full scale.  No
3.3 V-capable part reaches it; zero and span are calibrated downstream.
  THE TERM blocks.md's TABLE OMITS - RAIL SENSITIVITY.  The pedestal is a
  RATIO of the rail (0.2519/3.3 = 7.63 %) and reaches the output at gain 1,
  so dVout/dVs = 0.0763 V/V (bench B6 measures exactly that) = 548 uV RTI
  per volt of rail.  So 0.7 % of rail movement AFTER calibration - about
  9.1 mV on 3.3 V - eats the whole 5 uV budget on its own, the DOMINANT
  post-calibration term  ahead of the 1.1 uV R2/R3 ratio-TCR the table does
  count.  Not an error and not a scope miss to state: pedestal calibrates
  out; a voltage reference's stability is what matters, and it is on the
  +3V3 SOURCE, not on the divider.  Stated here so it is not lost.

(The "no output isolation resistor" result is recorded on the sheet itself,
beside the U2B -> J2 run where the part would have gone.)
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Title: **BP-amp bridge front end - AD8226 x OPA2333, G=139.2, 3.3V**