



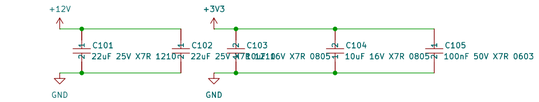


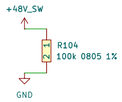
ai-ee

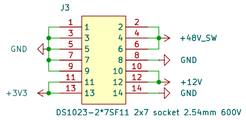
Sheet: /
File: PCB-0005-A_lumina-par.kicad_sch

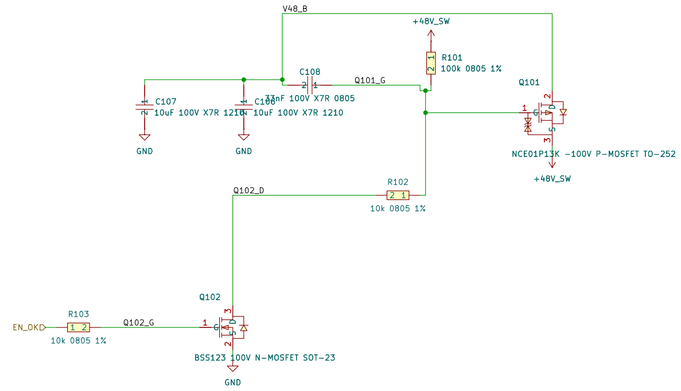
Title: LUMINA par LUM-PAR-A: root

Size: A4	Date: 2026-08-07	**Rev: 1**
KiCad E.D.A. 10.0.6		Id: 1/6









J3 PIN NUMBERS: ICD-01 s3.1 ONLY.

The DS1023 datasheet publishes none.

Bottom side, reverse-mounted, facing down

(ICD s7.3) — side is set at P6, and pin 1

must be checked in the MATED view, not

from the footprint.

+48V_SW IS LANDED, NOT TAPPED (branch A).

J3 1/3/5 -> TP103 + DNP bleed R104, and

stops. No 48 V bulk is stored, so

CAR-REQ-17 is not triggered: R104 exists

so it is met the instant any is added.

0.635 mm outer clearance, board-wide, on

every 48 V net (ICD s5.4).





TEST POINTS CARRY THE ICD s9 BENCH-HAZARD

SILKSCREEN. The fixture floats at PoE

potential; an earthed probe breaks PD

signature detection outright. Silk text is

a P6/P7 place_edit add_text op.

THIS SHEET OWNS THE PWR_FLAGS for GND,

+12V, +3V3 and +48V_SW. Every rail enters

through J3's passive pins. Do NOT add a

second flag on another sheet: PWR_FLAG is

a power_out pin and two of them collide.

BRANCH-B FRONT END (Q101/Q102/R101-R104/

C106-C108) IS DNP ON BRANCH A, and is in

the netlist on purpose — a DNP part still

has pads, so its clearance and area are

accounted for at P6/P7 and branch B stays

a populate change, not a respin.

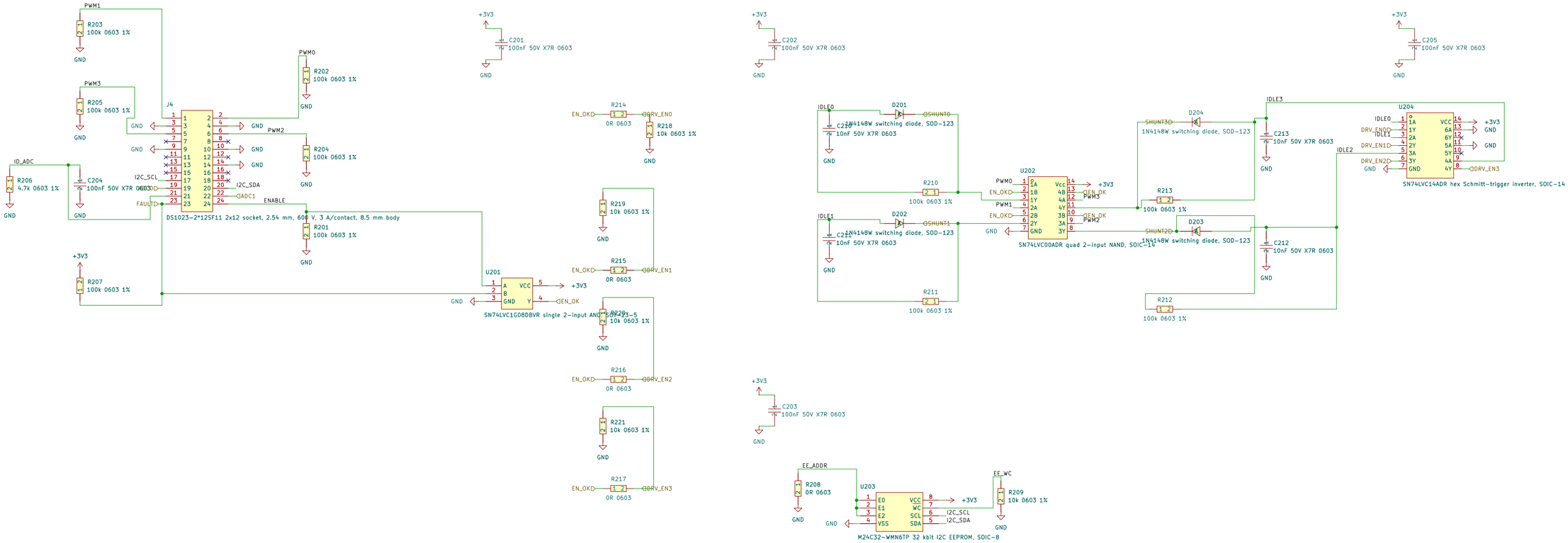
ai-ee

Sheet: /power/

File: power.kicad_sch

Title: LUM-PAR-A: power — J3 rail entry, bulk, test points, branch-B front e

Size: A2	Date: 2026-08-07	**Rev: 1**
KiCad E.D.A. 10.0.6		Id: 2/6



NO I2C PULL-UPS ON THIS BOARD (ICD-01 s3.3): the carrier fits the only 4.7 k pair. A second pair here is an ICD violation.

/FAULT IS OPEN DRAIN AND MUST NEVER BE DRIVEN HIGH. Its only drivers are the thermal sheet's LM339LV open-drain outputs and R207.

NO RC FILTER ON PWM0-3 OR /SHUNT0-3 (blocks.md B2): tau <= 14 ns if any network is fitted at all. The reflex 1 k + 100 pF is tau = 100 ns.

PWM4-7 (J4 7/8/11/12) and DSPI_SCK/MOSI/MISO/CSn (J4 14/15/16/17) are DELIBERATE no-connects - rev A has four channels (decisions.md D2).

R206 = 4.7 kOhm 1% REQUIRED: ICD-01 s3.4 code 2 (LUM-PAR-A). V_ID = 1.055 V. CR-1 CLOSED - sheets.md's 'VALUE TBD / P4 blocker' is STALE.

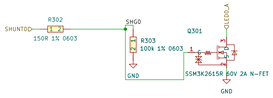
U203 = M24C32 at 0x50: E0/E1/E2 strapped to VSS by R208. WC (pin 7) is ACTIVE HIGH write protect - R209 holds it at VSS so the part is writable.

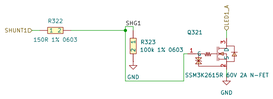
U204 + R210-R213 + C210-C213 + D201-D204 = converter-idle one-shot, DNP OPTION. IF IT IS EVER POPULATED, REMOVE R214-R217.

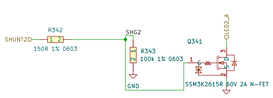
J4 IS REVERSE-MOUNTED ON THE BOTTOM SIDE, FACING DOWN (ICD s7.3). Pin 1 needs a silkscreen triangle and MUST be checked in the MATED view.

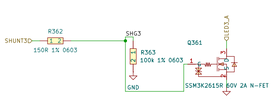
R218-R221 = 10k /DRV_ENn pull-downs, FITTED. NOT 100k: the TPS92515HV PWM pin sources 25 uA, so 100k rests at 2.5 V and latches the driver ON.

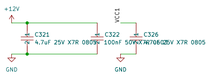
ai-ee		
Sheet: /control/		
File: control.kicad_sch		
Title: LUM-PAR-A: control - ENABLE gating, shunt logic, ID + EEPROM		
Size: A2	Date: 2026-08-07	**Rev: 1**
KiCad E.D.A. 10.0.6		Id: 3/6





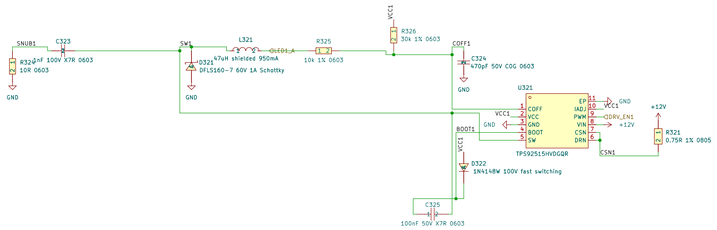


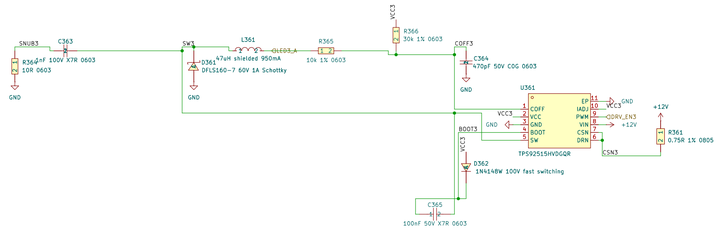




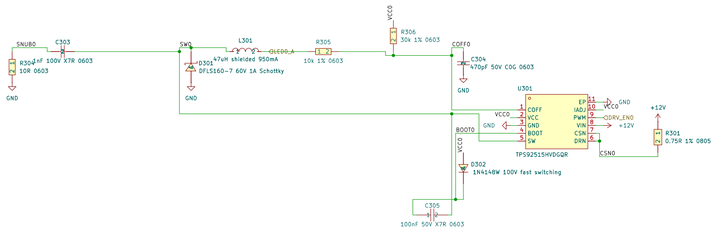


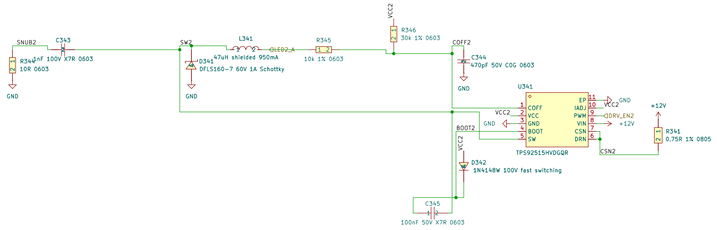












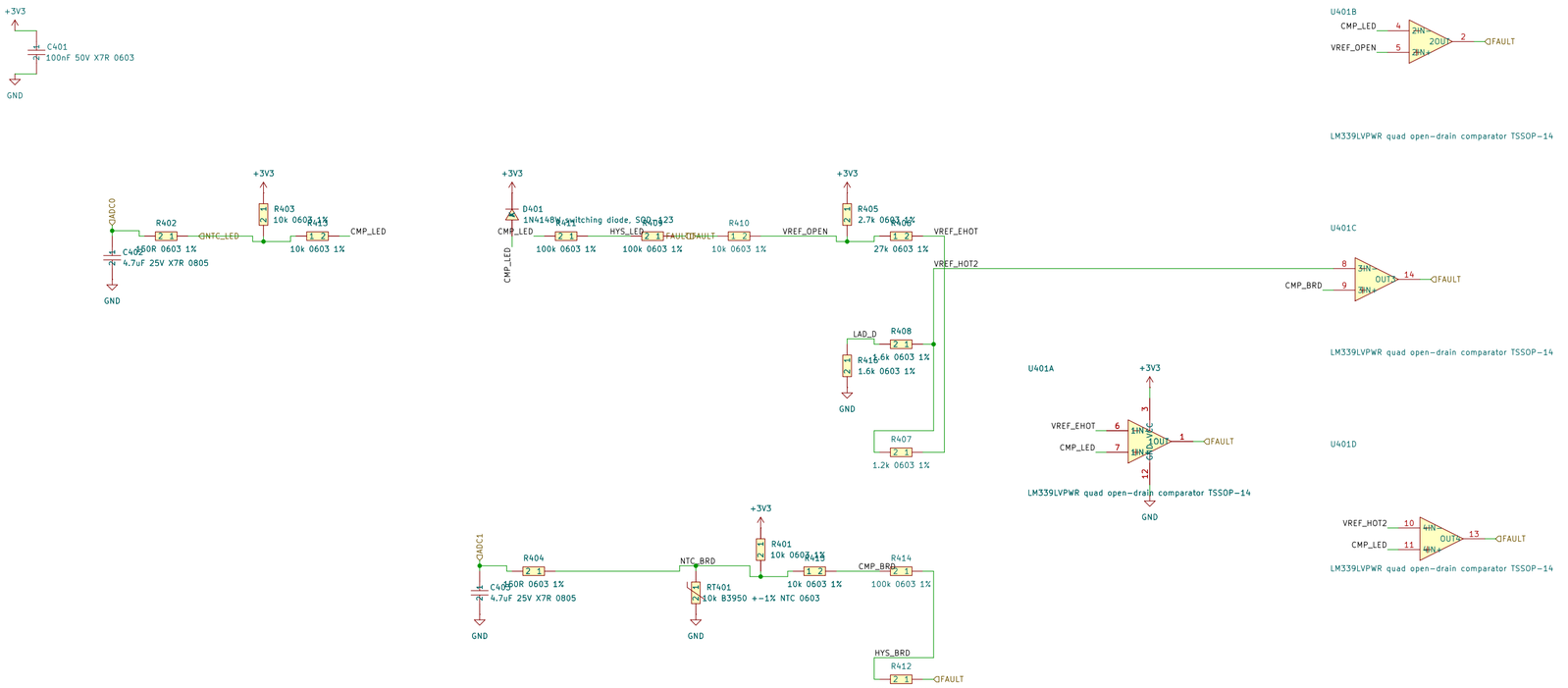
al-ee

Sheet: /drivers/

File: drivers.kicad_sch

Title: LUM-PAR-A: drivers (4x TPS92515HV CC buck + shunt FET)

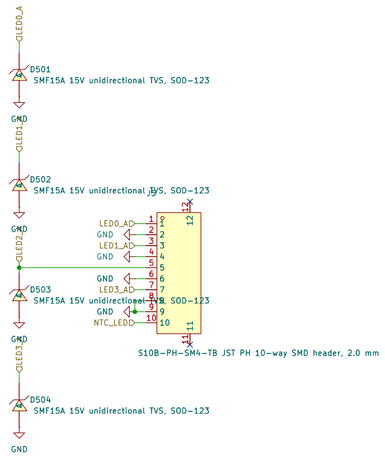
Size: A1	Date: 2026-08-07	**Rev: 1**
KiCad E.D.A. 10.0.6		Id: 4/6

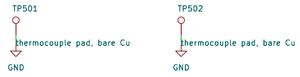


HYSTERESIS RETURNS TO CMP_LED / CMP_BRD, NOT to the divider nodes. On the divider the emitter-OPEN channel gets NET NEGATIVE feedback and oscillates between Rntc 110k and 200k — a fracturing crimp passes through that window. R410 = 10k is the open channel's ONLY positive path.

U401 INPUT PROTECTION (R413/R415 + D401): LM339LV inputs are abs-max 6 V and are clamped to GND ONLY — there is no ESD clamp to V+. /NTC_LED shares the J5 harness with LED anodes that reach the SMF15A 16.7–24.4 V clamp region. Series R alone does NOTHING without D401. DO NOT REMOVE EITHER, and keep D401's band toward +3V3.

ai-ee		
Sheet: /thermal/		
File: thermal.kicad_sch		
Title: LUM-PAR-A: thermal (NTC dividers, window comparator, FAULT)		
Size: A2	Date: 2026-08-07	**Rev: 1**
KiCad E.D.A. 10.0.6		Id: 5/6





J5 IS SIDE ENTRY AND ITS LAND IS ASYMMETRIC: the two solder tabs sit 0.2 mm beyond the wafer's MATING end face, the 10 circuit pads 5.5–9.0 mm behind it. P6 must point that end face OUT across the top edge and must NOT mirror the footprint — mirrored puts the opening on the wrong side of the edge. Check it in the MATED view, as ICD s7.2 requires for J3/J4.

PIN 9 IS A DEDICATED NTC SENSE RETURN. It is GND in the netlist and there is no way to say more there, so P6/P7 owns it: pin 9's copper must reach GND at the analogue reference point near U401, NOT be stitched into the plane at the connector (blocks.md B6). No gate enforces this.

TP501/TP502 CARRY THE ICD s9 BENCH-HAZARD SILKSCREEN. These are BARE-COPPER pads on GND, and this board's GND floats at PoE potential: an earthed scope probe or a non-isolated USB-UART adapter ties it to earth and BREAKS PD SIGNATURE DETECTION outright (detection is a few hundred uA), on top of the shock and damage risk. Probe only through an isolated instrument. Silk text is a P6/P7 place_edit add_text op.

ai-ee

Sheet: /led_if/

File: led_if.kicad_sch

Title: LUM-PAR-A: led_if — J5 LED harness, TVS clamps, TC pads (B6)

Size: A2	Date: 2026-08-07	**Rev: 1**
KiCad E.D.A. 10.0.6		Id: 6/6